

Application No.: 10/782,369

Docket No.: JCLA12973

**REMARKS****Present Status of the Application**

The Office Action rejected claims 1-2 and 4-5 under 35 U.S.C. 102(e), as being anticipated by Applicant Admitted Prior Art (AAPA). The Office Action also rejected claims 3 and 6-7 under 35 U.S.C. 103(a), as being unpatentable over AAPA in view of Hopewell et al. (U.S. 5,124,927). Applicants have amended claims 1 and 4 to improve clarity. After entry of the foregoing amendments, claims 1-7 remain pending in the present application, and reconsideration of those claims is respectfully requested.

**Summary of Applicant's Invention**

The Applicant's invention is directed to a method for forming a patterned photoresist layer. In the present invention, **right after the photoresist is exposed to form a latent image in the photoresist, the overlay offset between the latent image and the predetermined layer is measured.** Since the overlay measurement is performed right after the exposure step and before the development step in this invention, the overlay offset can be fed back in real time to avoid undesired rework.

Application No.: 10/782,369

Docket No.: JCLA12973

**Discussion of Office Action Rejections**

*The Office Action rejected claims 1-2 and 4-5 under 35 U.S.C. 102(e), as being anticipated by Applicant Admitted Prior Art (AAPA) and asserted that AAPA discloses all claimed features of the present invention.*

Applicants respectfully traverse the rejections for at least the reasons set forth below.

It is well established that anticipation under 35 U.S.C. 102 requires each and every elements of the rejected claims must be disclosed exactly by a single prior art reference.

The amended independent claims 1 and 4 are allowable for at least the reason that AAPA fails to teach or disclose each and every features of the amended independent claims 1 and 4. AS amended, claims 1 and 4 recite respectively:

Claim 1. A method for forming a patterned photoresist layer, being used to form a patterned photoresist layer aligned with a predetermined wafer layer and comprising:

- (a) forming a photoresist layer on a substrate;
- (b) exposing the photoresist layer;
- (c) **measuring an overlay offset between exposed portions of the photoresist layer and the predetermined layer right after the photoresist layer is exposed;**
- (d) determining whether the overlay offset is acceptable or not; and
- (e) developing the photoresist layer if the overlay offset is acceptable.

Claim 4. A method for forming a patterned photoresist layer, being used to form a patterned photoresist layer aligned with a predetermined wafer layer and comprising:

- (a) forming a photoresist layer on a substrate;
- (b) using an exposure/overlay-measurement tool to expose the photoresist layer to form a latent image in the photoresist layer;
- (c) **using the exposure/overlay-measurement tool to measure an overlay offset between the latent image and the predetermined layer right after the latent image is formed;**
- (d) comparing the overlay offset with a predetermined value; and
- (e) developing the photoresist layer if the overlay offset is smaller than the predetermined value.

Application No.: 10/782,369

Docket No.: JCLA12973

*(Emphasis added)*. Applicants submit that claims 1 and 4 patently define over the cited arts for at least the reason that the cited art fails to disclose at least the features emphasized above.

More specifically, AAPA fails to teach or suggest that the overlay offset is measured before the photoresist layer is developed. In AAPA, as shown in Fig. 1 of the present invention, the overlay offset between the developed photoresist layer and the predetermined layer is measured right after the exposed photoresist layer is developed. Apparently, in AAPA, while the overlay offset is not within a tolerable range, the developed photoresist layer is removed and a new photoresist is formed over the substrate. That is, while the developed photoresist layer is not sufficiently aligned with the predetermined layer, the developed photoresist layer is removed for rework with referring to the overlay offset measurement result (paragraph [0005]).

In the present invention, since the exposure step and the overlay measurement step are done in the same tool, the cycle time in the lithography process can be reduced. Furthermore, the overlay measurement is performed right after the exposure step and before the development step, so that the overlay offset can be real-time fed back to the exposure module to avoid undesired rework. Moreover, the overlay measurement is performed before the development step, the accuracy of the measurement result is relatively better without being affected by the development step.

Hence, Applicants respectfully submit that AAPA substantially fails to teach each and every feature of claims 1 and 4, and therefore, AAPA cannot possibly anticipate the claimed invention as claimed in the proposed independent claims 1 and 4 in this regard. Furthermore,

**Application No.: 10/782,369**

**Docket No.: JCLA12973**

skilled artisan would not modify AAPA to obtain the same advantage as what claimed by the present invention because AAPA never teaches or implies that the overlay measurement is performed right after the photoresist layer is exposed to form the latent image therein. Therefore, AAPA fails to render the present invention unpatentable.

Claims 2 and 5, which depend from claims 1 and 4 respectively, are also patentable over AAPA, at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 1-2 and 4-5 patently define over AAPA, and therefore should be allowed. Reconsideration and withdrawal of the above rejections is respectfully requested.

*The Office Action also rejected claims 3 and 6-7 under 35 U.S.C. 103(a), as being unpatentable over AAPA in view of Hopewell et al. (U.S. 5,124,927).*

Since claims 3 and 6-7 are dependent claims which further define the invention recited in claims 1 and 4 respectively, Applicants respectfully assert that these claims also are in condition for allowance according to the same reasons as discussed above for the rejection 102. Thus, reconsideration and withdrawal of this rejection are respectfully requested.

Application No.: 10/782,369

Docket No.: JCLA12973

**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims 1-7 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: 10/5/2005

4 Venture, Suite 250  
Irvine, CA 92618  
Tel.: (949) 660-0761  
Fax: (949)-660-0809

Respectfully submitted,  
J.C. PATENTS

  
Jiawei Huang  
Registration No. 43,330